BUFFERED FINFET DEVICE

BACKGROUND

1. Technical Field

The present invention relates generally to integrated circuit devices.

2. Description of the Background Art

FinFET (fin field effect transistor) devices are non-planar transistor devices which have been developed relatively recently. FinFET devices are generally characterized by a vertical fin-shaped channel and are typically formed on silicon-on-insulator (SOI) or bulk silicon substrates.

It is highly desirable to improve the robustness of finFET devices.

SUMMARY

One embodiment relates to a buffered transistor device. The device includes a buffered vertical fin-shaped structure formed in a semiconductor substrate. The vertical fin-shaped structure includes at least an upper semiconductor layer, a buffer region, and at least part of a well region. The buffer region has a first doping polarity, and the well region has a second doping polarity which is opposite to the first doping polarity. At least one p-n junction that at least partially covers a horizontal cross section of the vertical fin-shaped structure is formed between the buffer and well regions.

Other embodiments, aspects and features are also disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a flow chart of a method of fabricating a buffered finFET device in accordance with an embodiment of the invention.

FIG. **2** is a planar view showing select features of a buffered finFET device in accordance with an embodiment of the invention.

FIG. **3** shows three cross-sectional views of a first device structure after the patterning of resist on a hard mask layer in accordance with an embodiment of the invention.

FIG. **4** shows three cross-sectional views of the first device structure after an oxide fill and chemical-mechanical planarization in accordance with an embodiment of the invention.

FIG. **5** shows three cross-sectional views of the first device structure after source-drain extension implantation in accordance with an embodiment of the invention.

FIG. **6** shows three cross-sectional views of the first device structure after the fabrication process in accordance with an embodiment of the invention.

FIG. **7** is a planar view showing select features of a buffered finFET device and a neighboring well tap in accordance with an embodiment of the invention.

FIG. **8** shows a cross-sectional view after various steps during the fabrication of the buffered finFET device and the neighboring well tap in accordance with an embodiment of the invention.

FIG. **9** shows three cross-sectional views of the second device structure after the fabrication process in accordance with an alternate embodiment of the invention.

FIG. **10** is a simplified partial block diagram of a field programmable gate array (FPGA) that may be configured to implement an embodiment of the present invention.

FIG. **11** shows cross-sectional views of a device structure with a p-n junction which only partially spans a horizontal cross section of the vertical fin-shaped structure in accordance with an embodiment of the invention.

Note that the figures provided herewith are not necessarily to scale. They are provided for purposes of illustration to ease in the understanding of the presently-disclosed invention.

DETAILED DESCRIPTION

Applicants have determined that the extremely small dimensions of finFET devices in memory cells make the cells susceptible to single event upsets (SEUs) and electronic noise signals. SEUs may be caused by radiation causing the generation of electron-hole pairs at a sensitive node within a cell. The operation and performance of an integrated circuit may be substantially compromised by such SEUs. For example, field programmable gate arrays (FPGAs) and other programmable logic devices (PLDs) may be particularly sensitive to SEUs occurring in configuration random access memory (CRAM) cells. Other types of integrated circuits, such as microprocessors and application specific integrated circuits (ASICS), may also be sensitive to SEUs.

In addition, finFET devices are also susceptible to electronic noise signals which may be transmitted by way of conductive paths from other parts of an integrated circuit In particular, substrate noise may adversely impact the performance of a finFET device used in an analog circuit application.

The present disclosure provides a buffered finFET device and method of fabricating the device. In one example application, the buffered finFET device may be utilized in static memory cells so as to substantially reduce the occurrence of SEUs in the memory cells. For instance, the buffered finFET devices may be employed in CRAM cells in FPGAs or other integrated circuits. The noise resistant feature of the buffered finFET device also makes it less susceptible to substrate noise and hence well-suited for analog circuit applications.

FIG. **1** is a flow chart of a method **100** of fabricating a buffered finFET device in accordance with an embodiment of the invention. The fabrication method **100** is described below in conjunction with the structural diagrams in FIGS. **2** through **6**.

A top (plan) view showing select features and three cross-sectional planes of the buffered finFET device is given in FIG. **2**. Note that a primary purpose of FIG. **2** is to show the locations of the three cross-sectional planes which are used in the cross-sectional drawings of FIGS. **3-6** and **9**. The features depicted in FIG. **2** are actually buried beneath other layers in the final finFET device. The first cross-sectional plane in FIG. **2** is labeled A-A' and cuts across the three fins under the gate electrode **508**. In other words, the electrical current flowing through the fins when the transistor is on would flow through the A-A' plane. The second cross-sectional plane is labeled B-B' and is parallel to A-A'. The B-B' plane cuts across three drain (or source) features **512**. The third cross-sectional plane is labeled C-C' and is perpendicular to A-A' and B-B'. The C-C' plane cuts lengthwise though a fin.

FIGS. **3** through **6** depict cross-sectional views of a first device structure along the three cross-sectional planes (A-A', B-B', and C-C') at various points in the fabrication process in accordance with an embodiment of the invention. The fabricated device shown in FIG. **6** provides one p-n junction for radiation hardening (and noise isolation) between the channel and the base of the vertical fin-shaped structure.

FIG. **9** depicts cross-sectional views of a second device structure along the three cross-sectional planes (A-A', B-B', and C-C') after the fabrication process in accordance with an embodiment of the invention. The fabricated device shown in